Code.No: RR410505 | RR | SET-1

IV B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
VLSI SYSTEMS DESIGN
(COMMON TO CSE, CSS, ECC)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks
- - -

1. a) Explain why CMOS technology is most suitable for VLSI ICs?
   b) List the advantages and disadvantages of CMOS technology over bipolar technology. [8+8]

2. a) Define the following terms:
      i) Fan – out
      ii) Logic levels
      iii) Propagation delay
      iv) Noise margin
   b) Draw a stick diagram CMOS 2-input NAND gate. [8+8]

3. a) Draw a layout for CMOS 2-input NOR gate.
   b) Implement 2-input AND gate using static complementary logic. [8+8]

4. a) Compare dynamic and re-circulating latches.
   b) With example, explain what do you mean by transistor sizing? [8+8]

5. a) Explain the path-delay measurement of combinational logic circuits.
   b) Explain the design principles of pipelining. [8+8]

6. Explain about power distribution and clock distribution of routing procedure. [16]

7. Explain any one routing algorithm with suitable example. [16]

8. Write short notes on any TWO:
      i) FPGA
      ii) Hardware / software co – design
      iii) Architectural testing. [5+5+6]

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Code.No: RR410505 | RR | SET-2

IV B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
VLSI SYSTEMS DESIGN
(COMMON TO CSE, CSS, ECC)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks
- - -

1. a) Draw a layout for CMOS 2-input NOR gate.
   b) Implement 2-input AND gate using static complementary logic. [8+8]

2. a) Compare dynamic and re-circulating latches.
   b) With example, explain what do you mean by transistor sizing? [8+8]

3. a) Explain the path-delay measurement of combinational logic circuits.
   b) Explain the design principles of pipelining. [8+8]

4. Explain about power distribution and clock distribution of routing procedure. [16]

5. Explain any one routing algorithm with suitable example. [16]

6. Write short notes on any TWO:
   i) FPGA
   ii) Hardware / software co – design
   iii) Architectural testing. [5+5+6]

7. a) Explain why CMOS technology is most suitable for VLSI ICs?
   b) List the advantages and disadvantages of CMOS technology over bipolar technology. [8+8]

8. a) Define the following terms:
   i) Fan – out
   ii) Logic levels
   iii) Propagation delay
   iv) Noise margin
   b) Draw a stick diagram CMOS 2-input NAND gate. [8+8]

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Code.No: RR410505 | RR | SET-3

IV B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
VLSI SYSTEMS DESIGN
(COMMON TO CSE, CSS, ECC)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks
- - -

1. a) Explain the path-delay measurement of combinational logic circuits.
   b) Explain the design principles of pipelining. [8+8]

2. Explain about power distribution and clock distribution of routing procedure. [16]

3. Explain any one routing algorithm with suitable example. [16]

4. Write short notes on any TWO:
   i) FPGA
   ii) Hardware / software co – design
   iii) Architectural testing. [5+5+6]

5. a) Explain why CMOS technology is most suitable for VLSI ICs?
   b) List the advantages and disadvantages of CMOS technology over bipolar technology. [8+8]

6. a) Define the following terms:
   i) Fan – out
   ii) Logic levels
   iii) Propagation delay
   iv) Noise margin
   b) Draw a stick diagram CMOS 2-input NAND gate. [8+8]

7. a) Draw a layout for CMOS 2-input NOR gate.
   b) Implement 2-input AND gate using static complementary logic. [8+8]

8. a) Compare dynamic and re-circulating latches.
   b) With example, explain what do you mean by transistor sizing? [8+8]

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Code.No: RR410505 | RR | SET-4

IV B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
VLSI SYSTEMS DESIGN
(COMMON TO CSE, CSS, ECC)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks
- - -

1. Explain any one routing algorithm with suitable example. [16]

2. Write short notes on any TWO:
   i) FPGA
   ii) Hardware / software co – design
   iii) Architectural testing. [5+5+6]

3. a) Explain why CMOS technology is most suitable for VLSI ICs?
   b) List the advantages and disadvantages of CMOS technology over bipolar technology. [8+8]

4. a) Define the following terms:
   i) Fan – out
   ii) Logic levels
   iii) Propagation delay
   iv) Noise margin
   b) Draw a stick diagram CMOS 2-input NAND gate. [8+8]

5. a) Draw a layout for CMOS 2-input NOR gate.
   b) Implement 2-input AND gate using static complementary logic. [8+8]

6. a) Compare dynamic and re-circulating latches.
   b) With example, explain what do you mean by transistor sizing? [8+8]

7. a) Explain the path-delay measurement of combinational logic circuits.
   b) Explain the design principles of pipelining. [8+8]

8. Explain about power distribution and clock distribution of routing procedure. [16]

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